**Drawing Package Supplement**

to

**Centipede™**

**Operation, Maintenance and Service Manual**

**Contents of this Drawing Package**

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<td></td>
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</tbody>
</table>
British-Made Coin Door Schematic
Coin Door Schematic (037050-01 A)
Regulator Audio

Regulator/Audio II PCB

The Regulator/Audio II PCB has a regulator accurately regulating the logic power and an audio amplifier. The regulator II PCB by monitoring the voltage through the inputs +SENSE and -SENSE. The +5 VDC and ground inputs to the regulator regulates the voltage further in the harness between the regulator and the power. The resistor R8 is adjusted for the +5 VDC. Once adjusted, the voltage at the input remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between +5 VDC and ground of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio II PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 VDC and ground of the Regulator/Audio II PCB. Voltage should be greater than +5.5 VDC. If ground reading is less then 2 VDC, check connectors on both the game PCB and Regulator/Audio II PCB.
4. If cleaning PCB edge connectors does not correct for voltage difference, connect minus lead of voltmeter to T14 test point of Regulator/Audio II PCB and positive to GND test point of game PCB.

Audio Circuit

The audio circuit contains two inverters. Each amplifier consists of a T14 with an effective gain of 2.2.
dual functions of reg

game PCB and am-

regulator Q1, power resistor Q2. The regulator input to the game with high-impedance inputs are directly from game PCB. Therefore, the game PCB. This IR loss in the wire game PCB. Variable DC on the game PCB. AC of the game PCB.

J and GND test points

the Regulator/Audio II
voltmeter.
V REG and GND on
age reading must not ter, try cleaning edge PCB and the Regula-
doesn't decrease volt-
d of voltmeter to GND PCB and plus lead to rate the voltage.
eter to +5 REG test
nd plus lead to +5 V
is you can see which voltage. Troubleshoot harness connector.

dependent audio ampli-
2002AV amplifier with

a test point

American-Made Co
## Diagnostic Tests

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Use of Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Hold the slam switch closed, while setting the self-test switch to the on position.</td>
<td>The monitor displays the color hue adjustment pattern of 16 rectangles, as follows. Do not attempt any color hue or brightness adjustments unless you are a qualified color TV technician!</td>
</tr>
<tr>
<td>Pale Yellow-Green</td>
<td>Orange</td>
</tr>
<tr>
<td>Light Green</td>
<td>Dark Green</td>
</tr>
<tr>
<td>Deep Rose</td>
<td>Red</td>
</tr>
<tr>
<td>Navy Blue</td>
<td>Black</td>
</tr>
<tr>
<td>2. Activate any of the coin switches on the coin door.</td>
<td>A convergence pattern appears with a grid of white dots on a black screen. Do not attempt any convergence adjustments unless you are a qualified color TV technician!</td>
</tr>
<tr>
<td>3. Set self-test switch to the off position.</td>
<td>Check attract-mode display and readjust brightness if necessary.</td>
</tr>
</tbody>
</table>

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Power Input

Testing the CAT Box

1. Perform the CAT Box test.

2. Set the CAT Box to the following:
   a. Press TEST.
   b. BUS SOURCE
   c. BYTES to 10
   d. R/W MODE
   e. R/W to WRITE
   f. Key in 0000
   g. Toggle R/W to READ
   h. Toggle R/W to WRITE

3. If the CAT Box COMPARE ERROR shows the failure, repeat the test with the PLAY switch in.

4. If the COMPARE ERROR shows GOOD, repeat the test with the COMPARE ERROR in.

Denotes a test point
RAM

0x™ preliminary set-up.

Selects as follows:

RESET
TO ADDR
OFF

DE to SINGLE
DE to SINGLE

If an address that doesn't compare, the COM-

PROM lights, the ADDRESS/SIGNATURE display
address location, and the ERROR DATA Dis-

abled.

RROR LED does not light, rekey 0000 and re-

tach DBUS SOURCE switch set to ADDR. This

data bits at address 0000 will go high. If the

LED does not light after this step, the RAM

ROM
## Memory Map

<table>
<thead>
<tr>
<th>HEXA-DECIMAL ADDRESS</th>
<th>R/W</th>
<th>DATA (D7 D6 D5 D4 D3 D2 D1 D0)</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000-03FF</td>
<td></td>
<td>D D D D D D D D D D D D D D D</td>
<td>RAM</td>
</tr>
<tr>
<td>0400-07BF</td>
<td></td>
<td>D D D D D D D D D D D D D D D</td>
<td>Playfield RAM</td>
</tr>
<tr>
<td>07CC-07CF</td>
<td></td>
<td>D D D D D D D D D D D D D D D</td>
<td>Motion Object Picture</td>
</tr>
<tr>
<td>07D0-07DF</td>
<td></td>
<td>D D D D D D D D D D D D D D D</td>
<td>Motion Object Vert.</td>
</tr>
<tr>
<td>07E0-07EF</td>
<td></td>
<td>D D D D D D D D D D D D D D D</td>
<td>Motion Object Horiz.</td>
</tr>
<tr>
<td>07F0-07FF</td>
<td></td>
<td>D D D D D D D D D D D D D D D</td>
<td>Motion Object Color</td>
</tr>
<tr>
<td>0800</td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Option Switch 1 (0 = On)</td>
</tr>
<tr>
<td>0801</td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Option Switch 2 (0 = On)</td>
</tr>
<tr>
<td>0C00</td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Horizontal Trak Ball™ Inputs</td>
</tr>
<tr>
<td>0C01</td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>VBLANK (1 = VBlank)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Self-Test (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Cocktail Cabinet (1 = Cocktail)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>R,C,L Coin Switches (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>SLAM (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Player 2 Fire Switch (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Player 1 Fire Switch (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Player 2 Start Switch (0 = On)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Player 1 Start Switch (0 = On)</td>
</tr>
<tr>
<td>0C02</td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Vertical Trak Ball™ Inputs</td>
</tr>
<tr>
<td>0C03</td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Player 1 Joystick (R, L, Down, Up)</td>
</tr>
<tr>
<td></td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Player 2 Joystick (0 = On)</td>
</tr>
<tr>
<td>1000-100F</td>
<td>R/W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Custom Audio Chip</td>
</tr>
<tr>
<td>1404</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Playfield Color RAM</td>
</tr>
<tr>
<td>140C</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Motion Object Color RAM</td>
</tr>
<tr>
<td>1600</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>EA ROM Address &amp; Data Latch</td>
</tr>
<tr>
<td>1680</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>EA ROM Control Latch</td>
</tr>
<tr>
<td>1700</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>EA ROM Read Data</td>
</tr>
<tr>
<td>1800</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>IRQ Acknowledge</td>
</tr>
<tr>
<td>1C00</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Left Coin Counter (1 = On)</td>
</tr>
<tr>
<td>1C01</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Center Coin Counter (1 = On)</td>
</tr>
<tr>
<td>1C02</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Right Coin Counter (1 = On)</td>
</tr>
<tr>
<td>1C03</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Player 1 Start LED (0 = On)</td>
</tr>
<tr>
<td>1C04</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Player 2 Start LED (0 = On)</td>
</tr>
<tr>
<td>1C07</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Trak Ball™ Flip Control (0 = Player 1)</td>
</tr>
<tr>
<td>2000</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>WATCHDOG</td>
</tr>
<tr>
<td>2400</td>
<td>W</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Clear Trak Ball™ Counters</td>
</tr>
<tr>
<td>2000-3FFF</td>
<td>R</td>
<td>D D D D D D D D D D D D D D D</td>
<td>Program ROM</td>
</tr>
</tbody>
</table>
Signature Analysis Procedure

1. Perform the CAT Box™ preliminary set-up.

2. Connect the three BNC to E-Z clip cables (supplied with the CAT Box) to the SIGNATURE ANALYSIS CONTROL START, STOP, AND CLOCK jacks on the CAT Box.

3. Attach the three black E-Z clips to a ground loop on the CENTI-PEDET™ game PCB.

4. Attach the CAT Box data probe to the DATA jack on the CAT Box.

5. The red E-Z clips on the cables will be moved about for each group of signatures to be taken. The set-up for each group of signatures is located on the schematic sheet near the device to be checked. The signatures are located on or near the signal point on the schematic.

Note the example:

<table>
<thead>
<tr>
<th>IC#</th>
<th>PIN#</th>
</tr>
</thead>
<tbody>
<tr>
<td>SET-UP</td>
<td>SLOPE</td>
</tr>
<tr>
<td>START P2 11</td>
<td></td>
</tr>
<tr>
<td>STOP P2 11</td>
<td></td>
</tr>
<tr>
<td>CLK N1 6</td>
<td></td>
</tr>
</tbody>
</table>

6. Set the CAT Box switches as follows:
   a. TESTER MODE: SIG
   b. TESTER SELF TEST: OFF
   c. PULSE MODE: LATCHED
   d. START:
   e. STOP:
   f. CLOCK:
Preliminary Set-up

1. Power from the game.
2. Press from the game PCB.
3. From the cabinet.
4. From the game PCB.
5. Connectables to the game PCB and the wiring harness.
6. MPU socket with a piece of 28 AWG wire.
7. Cable to the game PCB test edge connector.
Sheet 2, Side A

Centipede™

Playfield Address Selector
Playfield Memory
Playfield Multiplexer
Picture Data ROM Circuitry
Motion Object Circuitry (Vertical)
Motion Object Circuitry (Horizontal)

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Motion Object Circuitry (Vertical)

The Motion Object Circuitry (vertical) receives playfield data and sync generator circuitry to generate the vertical component of the motion 15 from the playfield memory and 1V-128V from the sync generator area. The output is gated by A7 when a motion object is on one of the six latched by E6 to AND gate B7. A low on B7 pin 8 indicates the presence one of the vertical lines during non-active video time. This signal (MA)plexers in the picture data circuitry.

When 256H on pin 1 of D7 goes high, 1V, 2V, 4V and PIC0 are selected the latched output of E6 is selected. The output of D7 is EXCLUSIVE sent to the picture data selector circuitry as motion graphic address input to EXCLUSIVE OR gate E7 is PIC7 from the playfield code memory when high causes the output of E7 to be complemented. For example, PIC7 causes MGA0-MGA3 to go high. This causes the motion object to bottom.
Motion Object Circuitry (Horizontal)

The motion object circuitry (horizontal) receives playfield data and horizontal sync generator circuitry. PFD16-PFD23 from the playfield memory determine position of the motion object. PFD24-PFD29 from the playfield memory determine color of the motion object. PFD16-PFD23 are latched by L7 and loaded into the horizontal counters A5 and B5 by a low on pin 9. The horizontal position counters then RAMs A6 and B6. These RAMs are loaded with the video data for the particular bar from shift registers H9 and J9 (which were loaded from the graphics ROM). The RAMs A6 and B6 is then sent to the color PROM circuitry as MR0 and MR1.
playfield code multiplexer, MGA0-MGA3 (motion graphics address) from the motion object circuitry, 256H and 256H from the sync generator. PIC0-PIC5 represent the code for the object to be displayed. MGA0-MGA3 set one of eight different combinations of the 8-line by 8-bit blocks of picture video or the 16 line by 8 bit blocks of motion object video.

256H when high selects the playfield picture color codes to be addressed. 256H when low selects the motion object color codes to be addressed. The picture data ROM output D1-D8 on F7 and H/J7 are multiplexed by F6, H8, J8 and K8 and shifted out serially at H9 and J9. This serial output is latched by F9 as AREA0 and AREA1 to the motion object horizontal circuitry and the video output circuit.
Playfield Address Selector

The Playfield Address Selector controls the access to the playfield memory. It allows either the game MPU or the sync generator to scan the playfield memory. The Playfield Address Selector consists of multiplexers P5, and P7 and gate K4.

When 4H on pin 1 of P5 and P7 is low and pin 15 on P7 is low, the Playfield Address Selector receives 8H, 16H, 32H, and 64H on P5 and 16V, 32V, 64V, and 128V on P7 from the sync generator. These signals enable the sync generator circuits to access the playfield memory.

When 4H goes high the game MPU addresses the playfield memory (via AB0-AB9) for the positioning of the graphics. During horizontal blanking (pin 15 of P7 is high) the outputs of P7 (PFA4-PFA7) are held high enabling the motion object circuitry to access the playfield memory for the motion objects to be displayed.
3. If the CAT Box reads an address that doesn’t compare, the COMPARE ERROR LED lights, the ADDRESS/SIGNATURE display shows the failing address location, and the ERROR DATA DISPLAY switch is enabled.

4. If the COMPARE ERROR LED does not light, rekey 0400 and repeat the test with the DBUS SOURCE switch set to ADDR. This ensures that the data bits at address 0400 will go high. If the COMPARE ERROR LED does not light after this step, the Playfield RAM is good.
Playfield Multiplexer

The Playfield Multiplexer receives playfield data from the playfield memory and the output (PF0-PF7) is a code that determines what is 1) displayed on the monitor, or 2) read or updated by the MPU. The Playfield Multiplexer selects multiplexers K6, L6, M6, N6 and P6.

When 4H is low and 4H is high, AB4 and AB5 from the MPU address bus is the same as from P6. This output is applied to multiplexers K6, L6, M6, and N6. When the MPU is accessing the playfield code multiplexer, the playfield code is selected. When 256H is high and 4H is low from the sync generator (128H and 8V) are the selected outputs. When 4H is high, the playfield codes that eventually are displayed on the monitor.

One code (PF0-PF7) are latched by J5 and J6 to the MPU data bus (J5) are data PROM circuitry (J6). When PFRD is low and 1H from the MPU goes high, the inputs on J5 (PF0-PF7) are latched out to the MPU via 4H on pin 11 of J6 goes high, the inputs (PF0-PF7) are latched to the OM circuitry.
Picture Data ROM Circuitry

The picture data ROM circuitry receives picture information, assigns a color code to the information and sends it to the color PROM circuitry. The picture data ROM circuitry consists of ROM devices F7 and H/7, multiplexers F8, H8, J8, K8, shift registers H9 and J9, and latch F9.
Testing the Option Switches

1. Perform the CAT Box preliminary set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to READ
   d. Key in address 0800 (N9) or 0801 (N8)
   e. R/W MODE to STATIC

3. Activate the switch while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the switch is operating properly.

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Sheet 2, Side B

Centipede™

Joystick Circuitry
Mini-Trak Ball™ Circuitry
Player Input Circuitry
Video Output Circuitry
Audio Output Circuitry
Coin Counter Output Circuitry
Option Input Circuitry
High Score Memory Circuitry

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Coin Counter Output Circuit

This circuit consists of coin counter drivers Q6, Q7, and Q8 and data latch M10. The circuit is addressed by the MPU on A80-AB2 and written by the MPU on data line DB7. When the input to a driver is clocked high, its collector goes low grounding the return of the coin counter in the coin door.

Mini-Trak Ball™ Circuitry

Testing the Mini-Trak Ball™ Inputs

1. Perform the CAT Box Preliminary Set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to READ
   d. Key in address 0C00 (vertical) or 0C02 (horizontal)
   e. R/W MODE to PULSE

3. Spin the Mini-Trak Ball™ while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the Mini-Trak Ball input is operating properly.
1. If A8 pin 11 is low, transistor Q5 conducts and draws current from COLOR 3. The result is a pale blue when COLOR 1 and COLOR 2 are off.

2. If A8 pin 10 is low, transistor Q4 conducts and draws current from COLOR 2. The result is a pale green when COLOR 1 and COLOR 3 are off.

---

**High Score Memory Circuitry**

The High Score Memory circuit stores the three best scores and other pertinent information. These scores are saved even if power is removed from the game. The High Score Memory circuit consists of an erasable reprogrammable ROM E5, latches E4, H4, J4, buffer H5 and timer A11.

A11 produces a 0-15V square wave at a 1V rate. This signal, when +15V, forward biases diode CR5 and allows capacitor C86 to charge to −29V. When the signal is 0V, CR5 is cutoff and CR4 is forward-biased which causes C84 to develop a charge. C84 charges to approximately −28V. This is the potential required for EAROM C0 to operate.

The MPU addresses the EAROM (AB0-AB5) when a low EADDR gates WRITE2 at gate A4. The trailing edge of the gated pulse latches the address information to the EAROM E5 via J4. Data is latched by H4 at the same time. The EAROM mode (read, write or erase) is determined by DB0-DB3 at latch E4. A low EACONTROL gates WRITE2 at gate A4. The trailing edge of this gated pulse latches the data into the EAROM E5 via latch H4.

Data is read from the EAROM when EAREAD on pin 1 of buffer H4 goes low.
Player Input Circuitry

Coin Counter Output Circuitry

From MPU Address Bus Sheet 1, Side B
Testing the Audio Outputs

1. Perform the CAT Box preliminary set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/W to READ
   d. Key in address 0C00 (self-test switch only) or 0C01 (all others).
   e. R/W MODE to STATIC

3. Activate the following player input switches, one at a time, while monitoring the DATA DISPLAY:
   a. Coin Right
   b. Coin Left
   c. SLAM
   d. FIRE
   e. START 1
   f. START 2

4. The DATA DISPLAY will change if the switches are operating properly.

   Denotes a test point

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
<th>RESULTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>100F</td>
<td>00</td>
<td>Pure tone is heard from channel 1 output. Channel 1 output is turned off.</td>
</tr>
<tr>
<td>100F</td>
<td>03</td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td>55</td>
<td>Pure tone is heard from channel 2 output. Channel 2 output is turned off.</td>
</tr>
<tr>
<td>1001</td>
<td>AF</td>
<td></td>
</tr>
<tr>
<td>1001</td>
<td>00</td>
<td>Pure tone is heard from channel 3 output. Channel 3 output is turned off.</td>
</tr>
<tr>
<td>1002</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>1003</td>
<td>AF</td>
<td>Pure tone is heard from channel 4 output. Channel 4 output is turned off.</td>
</tr>
<tr>
<td>1003</td>
<td>00</td>
<td></td>
</tr>
<tr>
<td>1004</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>1005</td>
<td>AF</td>
<td></td>
</tr>
<tr>
<td>1005</td>
<td>00</td>
<td></td>
</tr>
<tr>
<td>1006</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>1007</td>
<td>AF</td>
<td></td>
</tr>
<tr>
<td>1007</td>
<td>00</td>
<td></td>
</tr>
</tbody>
</table>

The video output circuit receives motion object, playfield, address and data inputs and produces a video output to be displayed on the game monitor. In order to read out of the color RAM, GRY0 and GRY1 from the motion object circuitry are multiplexed with AREA0 and AREA1 from the playfield circuit by E8. The output, selected by GRY0 or GRY1, is RAMA0-RAMA3 (RAM ADDRESS).

RAMA0-RAMA3 are applied to color RAM C8. The colors red, green, blue and an alternate color bit are outputs. The three color bits are latched by A8 as the game video in the three basic colors (or shades of gray in a black and white monitor). When the alternate color bit (C8 pin 11) is active, an alternate shade of blue or green is available.

The following conditions, along with the various combinations of COLOR 1 (red), COLOR 2 (green) and COLOR 3 (blue),